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PATENT APPLICATION

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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Peterson, et al.

Confirmation No.: 7545

Application No.: 10/631,160

Examiner: Patel, Niketa I.

Filing Date: July 31, 2003

Group Art Unit: 2181

Title: System and Method for Adaptive Buffer in a Memory Device Interface

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on January 2, 2007.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☒ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☒ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☐ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 620. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees.

Respectfully submitted,

Peterson, et al.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:	)	Confirmation No. 7545
Peterson, et al.	)	Group Art Unit: 2181
Serial No.: 10/631,160	)	Examiner: Patel, Niketa I.
Filed: July 31, 2003	)	HP Docket: 200207081-1 TKHR Docket: 50833-1510
For: **System and Method for Adaptive Buffer in a Memory Device Interface**	)	

APPEAL BRIEF UNDER 37 C.F.R. §1.192

Mail Stop Appeal Brief - Patents
Commissioner of Patents and Trademarks
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

This is an appeal from the decision of Examiner Niketa Patel, Group Art Unit 2181, mailed November 2, 2006, rejecting claims 1, 3-6, and 8-19 of the present application and making the rejection FINAL.

I. REAL PARTY IN INTEREST

The real party in interest of the instant application is Hewlett-Packard Development Company, a Texas Limited Liability Partnership having its principal place of business in Houston, Texas.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claim 1, 3-6, and 8-19 are pending in this application, and all claims were rejected by the FINAL Office Action and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

There have been no claim amendments made after the Final Office Action, and all amendments made before the Final Office Action have been entered. A copy of the current claims is attached hereto as Appendix A.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Embodiments of the claimed subject matter are illustrated in FIGs. 1A through 10 and are discussed in the specification at least in paragraphs [0019] through [0068].

Embodiments of the invention, such as those defined by claim 1, define a method comprising determining at least one characteristic (see e.g., at least Figs. 2A and 2B, p. 5, line 16 ~ bottom of p. 6 of the specification) of a first input/output (I/O) device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26) that is coupled to a memory device (see e.g., Fig. 1A, element 106, p. 3, lines 12-26) (see e.g., Fig. 1A, element 102, p. 3, lines 12-26), the memory device interface being configured to enable data transfers between the first I/O device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26) and a memory device (see e.g., Fig. 1A, element 104, p. 3, lines 12-26). The method

further comprises buffering data corresponding to the first I/O device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26) in a first portion of a buffer of the memory device interface (see e.g., Fig. 1A, element 104, p. 3, lines 12-26), a size of the first portion being responsive to the at least one characteristic of the first I/O device (see e.g., p. 5, line 23~ p. 6, line5), and determining at least one characteristic of a second I/O device (see e.g., p. 5, line 19, reciting multiple I/O devices 102) that is coupled to the memory device interface. In addition, the method comprises buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device.

Embodiments of the invention, such as those defined by claim 6, define a method allocating buffer capacity in a memory device interface (see e.g., Fig. 1A and FIG. 3, element 104, p. 3, lines 12-26) that is configured to transfer data between an input/output (I/O) device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26) and a memory device (see e.g., Fig. 1A, element 106, p. 3, lines 12-26). The method comprises buffering data received via a first data transfer link (see e.g., FIG. 3, element 301) in a first portion of a buffer of the memory device interface (see e.g., Fig. 1A, element 104, p. 3, lines 12-26) and buffering data received via a second data transfer link (see e.g., FIG. 3, element 301) in a second portion of the buffer, a buffering capacity of the first portion being different than a buffering capacity of the second portion. In accordance with the embodiments of claim 6, the buffering capacity of the first portion is responsive to at least one characteristic of a first I/O device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26)that provides data to the memory device interface (see e.g., Fig. 1A, element 104, p. 3, lines 12-26) via the first data transfer link (see

e.g., FIG. 3, element 301), and the buffering capacity of the second portion is responsive to at least one characteristic of a second I/O device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26)that provides data to the memory device interface via the second data transfer link (see e.g., FIG. 3, element 301).

Embodiments of the invention, such as those defined by claim 10, define a memory device interface (see e.g., Fig. 1A, element 104, p. 3, lines 12-26) that is configured to enable data transfers between an input/output (I/O) device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26). The memory device interface (see e.g., Fig. 1A, element 104, p. 3, lines 12-26) comprises a buffer (see e.g., Fig. 4A, element 405, p. 9, lines 1-24), a first plurality of registers (see e.g., Fig. 7, element 701-708, p. 12, lines 6-19) that are configured to enable the memory device interface (see e.g., Fig. 1A, element 104, p. 3, lines 12-26) to buffer in a first portion of the buffer data corresponding to a first I/O device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26), and a second plurality of registers (see e.g., Fig. 7, element 709-716, p. 12, lines 6-19) that are configured to enable the memory device interface (see e.g., Fig. 1A, element 104, p. 3, lines 12-26) to buffer in a second portion of the buffer data corresponding to a second I/O device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26), a size of the first portion of the buffer being different than a size of the second portion of the buffer.

Embodiments of the invention, such as those defined by claim 15, define a memory device interface (see e.g., Fig. 1A, element 104, p. 3, lines 12-26) comprising a buffer (see e.g., Fig. 4A, element 405, p. 9, lines 1-24), a first plurality of registers (see e.g., Fig. 7, element 701-708, p. 12, lines 6-19) that are configured to enable the memory device interface (see e.g., Fig. 1A, element 104, p. 3, lines 12-26) to buffer in a

first portion of the buffer (see e.g., Fig. 4A, element 405, p. 9, lines 1-24) data received via a first data transfer link (see FIG. 3, item 301), and a second plurality of registers (see e.g., Fig. 7, element 709-716, p. 12, lines 6-19) that are configured to enable the memory device interface (see e.g., Fig. 1A, element 104, p. 3, lines 12-26) to buffer in a second portion of the buffer data received via a second data transfer link (see FIG. 3, item 301), a size of the first portion of the buffer being different than a size of the second portion of the buffer.

Finally, embodiments of the invention, such as those defined by claim 19, define a system comprising means for determining at least one characteristic of a first input/output (I/O) device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26) that is coupled to a memory device interface (see e.g., Fig. 1A, element 104, p. 3, lines 12-26), the memory device interface (see e.g., Fig. 1A, element 104, p. 3, lines 12-26) being configured to enable data transfers between the I/O device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26) and a memory device (see e.g., Fig. 1A, element 106, p. 3, lines 12-26), means for buffering data (see e.g., Fig. 4A, element 405, p. 9, lines 1-24) corresponding to the first I/O device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26) in a first portion of a buffer of the memory device interface (see e.g., Fig. 1A, element 104, p. 3, lines 12-26), a size of the first portion being responsive to the at least one characteristic of the first I/O device, means for determining at least one characteristic of a second I/O device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26) that is coupled to the memory device interface, and means for buffering data (see e.g., Fig. 4A, element 405, p. 9, lines 1-24) corresponding to the second I/O device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26) in a second portion of the buffer (see e.g., Fig.

4A, element 405, p. 9, lines 1-24), a size of the second portion being responsive to the at least one characteristic of the second I/O device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The FINAL Office Action rejected claims 1, 3-6, 8-10, 12-15, and 17-19 under 35 U.S.C. §102(e) as allegedly anticipated by Boyle (U.S. patent 6,708,251).

The FINAL Office Action also rejected claims 11 and 16 under 35 U.S.C. § 103(a) as allegedly unpatentable over Boyle in view of Ward (U.S. patent 4,894,770).

VII. ARGUMENT

The Final Office Action rejected all pending claims. Applicant respectfully requests that the rejections be overturned for at least the following reasons.

Rejections of Claims Under 35 U.S.C. §102(e) Should be Overturned

Independent Claim 1 (and dependent claims 3-5)

Claim 1 recites:

> 1. A method comprising:
> determining at least one characteristic of a first input/output (I/O) device that is coupled to a memory device interface, the memory device interface being configured to enable data transfers between the first I/O device and a memory device;
> buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface, a size of the first portion being responsive to the at least one characteristic of the first I/O device;
> ***determining at least one characteristic of a second I/O device that is coupled to the memory device interface; and***

> ***buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device.***

(*Emphasis added.*) Claim 1 patently defines over the cited art for at least the reason that Boyle fails to disclose the features emphasized above.

The Office Action cites element 22 of Boyle as being the first I/O device, and element 24 as being the second I/O device. In addition, the Office Action relies on column 3, lines 45-62 of Boyle as teaching the claimed features of "determining at least one characteristic of a first input/output (I/O) device" and "determining at least one characteristic of a second I/O device." This portion of Boyle actually states:

> The disk controller 80 is responsive to the host commands 72 to selectively allocate at least a portion of the buffer memory 40 for the audiovisual data 54. The disk controller 80 is further responsive to the host commands 72 to selectively transfer the audiovisual data 54 from the audiovisual interface 50 to the buffer memory 40. The disk controller 80 is further responsive to the host commands 72 to selectively transfer the audiovisual data 54 from the buffer memory 40 to the disk 30 to be stored. In the embodiment schematically illustrated in FIG. 1, the host command interface 70 is further adapted to receive second data 74 from the host system 20, and the disk controller 80 is further responsive to the host commands 72 to selectively allocate at least a portion of the buffer memory 40 for the second data 74, selectively transfer the second data 74 from the host command interface 70 to the buffer memory 40, and selectively transfer the second data 74 from the buffer memory 40 to the disk 30 to be stored.

As can be readily verified, neither reference number 22 or 24 (the alleged first and second I/O devices) are referenced in this portion of Boyle. Accordingly, this portion of Boyle cannot properly teach what the Office Action alleges it to teach.

More specifically, this portion of Boyle states that the disk controller is "responsive to host commands 72 to selectively allocate at least a portion of the buffer memory." This is NOT the same as "determining at least one characteristic of a first I/O device...," which Applicants have specifically claimed. Likewise, this portion of Boyle further states that "the disk controller 80 is further responsive to the host commands 72 to selectively allocate at least a portion of the buffer memory 40 for the second data." Again, this is not the same as "determining at least one characteristic of a second I/O device...," which Applicants have specifically claimed.

Further still, in the cited portion of Boyle, the disk controller 80 is responsive to the same thing (i.e., host commands 72) for allocating both portions of the buffer memory. In contrast, claim 1 specifies that the respective sizes of the first and second portions of the buffer memory are "responsive to at least one characteristic" of the first and second I/O devices, respectively. Thus, claim 1 specifies two different criteria at being determined (i.e., a characteristic of the first I/O device and a characteristic of the second I/O device), which criteria are used to dictate the size of the first and second portions of the buffer for buffering the corresponding data. For at least this reason, the rejection of claim 1 should be overturned.

In addition to the foregoing, the Office Action also cited column 7, lines 8-19 of Boyle as allegedly teaching the claimed features of determining characteristics of the first and second I/O devices. In fact, this portion of Boyle actually states:

> In certain embodiments, the fractions of the buffer memory 40 allocated to the input audiovisual data portion 41 and the input second data portion 42 are dynamically adjusted to satisfy the memory requirements for the transfer of the data to the disk 30. For example, in instances where there is a large amount of audiovisual data 54 to be transferred from the

> audiovisual interface 50, but a relatively small amount of second data 74, the fraction of the buffer memory 40 allocated to the input audiovisual data portion 41 can be increased while the fraction of the buffer memory 40 allocated to the input second data portion 42 can be reduced.

Again, as can be readily verified, this cited teaching of Boyle does not teach the relevant claimed features. In this regard, while this portion of Boyle apparently teaches that the different portions of the buffer memory may be dynamically adjusted to satisfy the memory requirements for the transfer of the data to the disk, there is no teaching of determining characteristics of first and second I/O devices, which characteristics are used to dictate the size of the respective buffer portions.

For at least these reasons, the rejections of independent claim 1 are clearly misplaced, and the rejection of claim 1 should be overturned.

Claims 3-5 depend from claim 1, and therefore patently define over the cited art for at least the same reason.

Independent Claim 6 (and corresponding dependent claims)

The Office Action rejected claim 6 as allegedly anticipated by Boyle. Applicant respectfully requests that this rejection be overturned for at least the following reasons.

Independent claim 6 recites:

> 6. A method for allocating buffer capacity in a memory device interface that is configured to transfer data between an input/output (I/O) device and a memory device, the method comprising:
> buffering data received via a first data transfer link in a first portion of a buffer of the memory device interface;
> buffering data received via a second data transfer link in a second portion of the buffer, a buffering capacity of the first portion being different than a buffering capacity of the second portion; and
> ***wherein the buffering capacity of the first portion is responsive to at least one characteristic of a first I/O device that***

> ***provides data to the memory device interface via the first data transfer link, and the buffering capacity of the second portion is responsive to at least one characteristic of a second I/O device that provides data to the memory device interface via the second data transfer link.***

(*Emphasis added.*) Claim 6 patently defines over the cited art for at least the reason that Boyle fails to disclose the features emphasized above.

With respect to the portion of claim 6 emphasized above, the Office Action cited col. 7, lines 5-19, 37-43, 59-62 and col. 4, lines 32-60 as allegedly disclosing the emphasized features. These portions of Boyle actually state:

> As schematically illustrated in FIG. 1, upon allocation, the buffer memory 40 has an input audiovisual data portion 41 and an input second data portion 42. In certain embodiments, the fractions of the buffer memory 40 allocated to the input audiovisual data portion 41 and the input second data portion 42 are dynamically adjusted to satisfy the memory requirements for the transfer of the data to the disk 30. For example, in instances where there is a large amount of audiovisual data 54 to be transferred from the audiovisual interface 50, but a relatively small amount of second data 74, the fraction of the buffer memory 40 allocated to the input audiovisual data portion 41 can be increased while the fraction of the buffer memory 40 allocated to the input second data portion 42 can be reduced.
> ...
> By not transferring the audiovisual data 54 to and from the disk drive 10 over the host command interface 70, more bandwidth is available for the host commands 72 and second data 74. In embodiments in which a large amount of audiovisual data 54 is transferred, the use of the separate audiovisual interface 50 avoids problems due to the limited bandwidth of the host command interface 70.
> ...
> ... In certain embodiments, the sizes of these portions of the buffer memory 40 are dynamically adjusted by the disk controller 80 to optimize the performance of the disk drive 10 in response to buffer demands.
> ...
> In embodiments in which the host system 20 comprises an audiovisual source 22 and a host device 24, such as schematically illustrated in FIG. 2, the audiovisual interface 50 is connectable to the audiovisual source 22 and the host command interface 70 is connectable to the host device 24. The audiovisual source 22 and the host device 24 can each comprise a

> set-top box, a personal video recorder, or other source of audiovisual information. In certain embodiments, the audiovisual source 22 and the host device 24 comprise a common device (i.e., the audiovisual interface 50 and host command interface 70 are connectable to the same device), as schematically illustrated in FIG. 3. In certain other embodiments, the audiovisual source 22 is an audiovisual data service provider that supplies first data 52 comprising video programming to multiple users. Examples of such audiovisual data service providers include, but are not limited to, cable television systems and satellite systems. Alternatively, the audiovisual source 22 can provide first data 52 which comprises UHF or VHF broadcast signals using an antenna and a tuner. In still other embodiments, the audiovisual source 22 can be a video camera, a video cassette recorder, or the like, that provides first data 52 corresponding to home video programs which the user wants to upload to the disk drive 10. Persons skilled in the art recognize audiovisual sources 22 and first data 52 that are compatible with embodiments of the present invention. Although the audiovisual source 22 may advantageously be a separate device (e.g., a video camera), the audiovisual source 22 is considered to be part of the overall host system 20.

As can be readily verified, these portions of Boyle do not teach the claimed features. Of the above-quoted portions of Boyle, the most relevant to the claim language appears to be the portion that states "the sizes of these portions of the buffer memory 40 are dynamically adjusted by the disk controller 80 to optimize the performance of the disk drive 10 in response to buffer demands." However, claim 6 requires that "***the buffering capacity of the first portion is responsive to at least one characteristic of a first I/O device that provides data to the memory device interface***." (a similar feature is required for the second portion and second I/O device). Since the same sections of Boyle have been duplicatively cited for both of the claimed features (i.e., the buffering capacity of the first portion and the buffering capacity of the second portion),the undersigned fails to see how BOTH claimed features are taught in the cited passage of Boyle. In fact it doesn't. For at least this reason, the rejection is misplaced and should be overturned.

As claims 8-10 depend from independent claim 6, the rejections of these dependent claims should be overturned for at least the same reasons.

Independent Claim 10 (and corresponding dependent claims)

The Office Action rejected claim 10 as allegedly anticipated by Boyle. Applicant respectfully requests that this rejection be overturned for at least the following reasons.

Independent claim 10 recites:

> 10. A memory device interface that is configured to enable data transfers between an input/output (I/O) device, the memory device interface comprising:
> a buffer;
> ***a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data corresponding to a first I/O device***; and
> ***a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data corresponding to a second I/O device, a size of the first portion of the buffer being different than a size of the second portion of the buffer.***

(*Emphasis added.*) Claim 10 patently defines over the cited art for at least the reason that Boyle fails to disclose the features emphasized above.

With respect to the portion of claim 10 emphasized above, the Office Action cited figure 2, element 41 (first plurality of registers) and figure 2, element 42 (second plurality of registers), and col. 7, lines 5-19, 37-43, 59-62 and col. 4, lines 32-60 as allegedly disclosing the emphasized features.

First and foremost, elements 41 and 42 disclose an "Input Audiovisual Data Portion" and an "Input Second Data Portion." The Office Action, however, cited these items as disclosing the claimed "first plurality of registers" and "second plurality of

registers". Simply stated, this application of Boyle to claim 10 is fundamentally misplaced, and the rejection should be overturned for at least this reason.

The remaining cited portion of Boyle (as quoted in connection with claim 6) actually state:

> As schematically illustrated in FIG. 1, upon allocation, the buffer memory 40 has an input audiovisual data portion 41 and an input second data portion 42. In certain embodiments, the fractions of the buffer memory 40 allocated to the input audiovisual data portion 41 and the input second data portion 42 are dynamically adjusted to satisfy the memory requirements for the transfer of the data to the disk 30. For example, in instances where there is a large amount of audiovisual data 54 to be transferred from the audiovisual interface 50, but a relatively small amount of second data 74, the fraction of the buffer memory 40 allocated to the input audiovisual data portion 41 can be increased while the fraction of the buffer memory 40 allocated to the input second data portion 42 can be reduced.
> ...
> By not transferring the audiovisual data 54 to and from the disk drive 10 over the host command interface 70, more bandwidth is available for the host commands 72 and second data 74. In embodiments in which a large amount of audiovisual data 54 is transferred, the use of the separate audiovisual interface 50 avoids problems due to the limited bandwidth of the host command interface 70.
> ...
> ... In certain embodiments, the sizes of these portions of the buffer memory 40 are dynamically adjusted by the disk controller 80 to optimize the performance of the disk drive 10 in response to buffer demands.
> ...
> In embodiments in which the host system 20 comprises an audiovisual source 22 and a host device 24, such as schematically illustrated in FIG. 2, the audiovisual interface 50 is connectable to the audiovisual source 22 and the host command interface 70 is connectable to the host device 24. The audiovisual source 22 and the host device 24 can each comprise a set-top box, a personal video recorder, or other source of audiovisual information. In certain embodiments, the audiovisual source 22 and the host device 24 comprise a common device (i.e., the audiovisual interface 50 and host command interface 70 are connectable to the same device), as schematically illustrated in FIG. 3. In certain other embodiments, the audiovisual source 22 is an audiovisual data service provider that supplies first data 52 comprising video programming to multiple users. Examples of such audiovisual data service providers include, but are not limited to,

> cable television systems and satellite systems. Alternatively, the audiovisual source 22 can provide first data 52 which comprises UHF or VHF broadcast signals using an antenna and a tuner. In still other embodiments, the audiovisual source 22 can be a video camera, a video cassette recorder, or the like, that provides first data 52 corresponding to home video programs which the user wants to upload to the disk drive 10. Persons skilled in the art recognize audiovisual sources 22 and first data 52 that are compatible with embodiments of the present invention. Although the audiovisual source 22 may advantageously be a separate device (e.g., a video camera), the audiovisual source 22 is considered to be part of the overall host system 20.

As can be readily verified, these portions of Boyle do not teach the claimed features. Of the above-quoted portions of Boyle, the most relevant to the claim language appears to be the portion that states "the sizes of these portions of the buffer memory 40 are dynamically adjusted by the disk controller 80 to optimize the performance of the disk drive 10 in response to buffer demands." However, claim 10 requires that "***a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data corresponding to a first I/O device***," and "***a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data corresponding to a second I/O device, a size of the first portion of the buffer being different than a size of the second portion of the buffer.***" As noted in connection with claim 6, the cited portions of Boyle do not disclose both first and second I/O devices and a memory device having first and second portions that are buffered in accordance with characteristics of the first and second I/O devices. For at least this reason, the rejection is misplaced and should be overturned.

As claims 12-15 depend from independent claim 10, the rejections of these dependent claims should be overturned for at least the same reasons.

Independent Claim 15 (and corresponding dependent claims)

The Office Action rejected claim 15 as allegedly anticipated by Boyle. Applicant respectfully requests that this rejection be overturned for at least the following reasons.

Independent claim 15 recites:

> 15. A memory device interface comprising:
> a buffer;
> ***a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data received via a first data transfer link***; and
> ***a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data received via a second data transfer link, a size of the first portion of the buffer being different than a size of the second portion of the buffer.***

(*Emphasis added.*) Claim 15 patently defines over the cited art for at least the reason that Boyle fails to disclose the features emphasized above.

The features of claim 15 emphasized above are similar to the features emphasized in claim 10, and the cited portions of Boyle (applied to these claimed features) are the as those applied against the emphasized elements of claim 6. Therefore, the rejection of claim 10 should be overturned for the same reasons as the rejections of claim 6.

As claims 16-18 depend from independent claim 15, the rejections of these dependent claims should be overturned for at least the same reasons.

Independent Claim 19 (and corresponding dependent claims)

The Office Action rejected claim 19 as allegedly anticipated by Boyle. Applicant respectfully requests that this rejection be overturned for at least the following reasons.

Independent claim 19 recites:

> 19. A system comprising:
> means for determining at least one characteristic of a first input/output (I/O) device that is coupled to a memory device interface, the memory device interface being configured to enable data transfers between the I/O device and a memory device;
> means for buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface, a size of the first portion being responsive to the at least one characteristic of the first I/O device;
> ***means for determining at least one characteristic of a second I/O device that is coupled to the memory device interface; and***
> ***means for buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device.***

(*Emphasis added.*) Claim 19 patently defines over the cited art for at least the reason that Boyle fails to disclose the features emphasized above.

Again, the Office Action applied the same teachings of Boyle (col. 7, lines 5-19, 37-43, 59-62 and col. 4, lines 32-60) against the emphasized features of claim 19, as it applied against the corresponding features of the other independent claims. Applicant respectfully submits that this application of Boyle is misplaced, for the same reason that the corresponding application of Boyle to the other independent claims is misplaced.

Further still, with respect to claim 19, Applicant notes that the elements of claim 19 are set forth in means-plus-function format. Even though the elements may loosely correspond to the claim elements of claim 1, they cannot properly be construed coextensively. Instead, pursuant to 35 U.S.C. § 112(6), a claim element recited in

means-plus-function format "shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." 35 U.S.C. § 112, ¶ 6. The Federal Circuit has clearly endorsed this statutory mandate by holding that claims interpreted under 35 U.S.C. § 112, paragraph 6, are limited to the corresponding structure disclosed in the specification and it equivalents. *Kahn v. General Motors Corp.* 135 F.3d 1472, 45 U.S.P.Q.2d 1608 (Fed. Cir. 1998).

There should be no question but that the elements recited in claim 20 are to be construed pursuant to 35 U.S.C. § 112, paragraph 6. In *Greenberg v. Ethicon Endo-Surgical Inc.*, 91 F.3d 1580, 39 U.S.P.Q. 2d 1783 (Fed. Cir. 1996), the Federal Circuit stated that the use of "means for" language generally invokes 112(6). Indeed, only if means plus function claim elements recite sufficient structure to carry out the function are that taken out of the gambit of 35 U.S.C. § 112, paragraph 6. *Cole v. Kimberly-Clark Corp.*, 102 F.3d 524, 41 U.S.P.Q.2d 1001 (Fed. Cir. 1996).

Indeed, the Federal Circuit reiterated in *Sage Products, Inc. v. Devon Industries, Inc.*, 126 F.3d 1420, 44 U.S.P.Q.2d 1103 (Fed. Cir. 1998) that "the use of the word 'means,' which is part of the classic template for functional claim elements, gives rise to 'a presumption that the inventor used the term advisedly to invoke the statutory mandates for means-plus-function clauses." Ultimately, the Court in *Sage* construed the relevant claim elements under 35 U.S.C. § 112(6), because 'means' were recited, and the claim elements did not "explicitly recite[s] the structure, material, or acts needed to perform the [recited] functions. *Sage* at p. 1428. The Federal Circuit further acknowledged this presumption in *Al-Site Corp. v. VSI International, Inc.*, 174 F.3d 1308, 50 U.S.P.Q.2d 1161 (Fed. Cir. 1999).

Thus, claim elements expressed in "means" plus function format are construed as determined in accordance with 35 U.S.C. § 112, paragraph 6, as set forth above, and as further described in In re Donaldson 16 F.3d 1189, 29 U.S.P.Q.2d 1845 (Fed. Cir. 1994)(*en banc*). Therefore, the various means elements of claim 19 must be construed in accordance with the corresponding structure set forth in the present specification. In this regard, Applicants note that, in *In re Donaldson,* The Board of Patent Appeals and Interferences advanced the legal proposition that "limitations appearing in the specification are *not* to be read into the claims of an application." *In re Donaldson* at 1848. This argument, however, was rejected by the Federal Circuit, which held, as a matter of law, that "one construing means-plus-function language in a claim must look to the specification and interpret that language in light of the corresponding structure ... described therein, and equivalents thereof. *In re Donaldson* at 1848. Furthermore, the holding in *In re Donaldson* does not conflict with the principle that claims are to be given their broadest reasonable interpretation during prosecution. *In re Donaldson* at 1850.

Accordingly, the fact that the Office Action appears to have construed the claim elements of claim 19 to be co-extensive with the claim elements of the other independent claims, the rejection of claim 19 is erroneous, and should be overturned.

Additional Comments Regarding Propriety of Rejections

In addition to the substantive comments above, the undersigned also notes that a pre-appeal conference request was made in this application noting that, due to the premature FINALity of the FINAL Office Action, the Applicants had not been given a fair

opportunity to develop clear issue in the prosecution of this application (required by MPEP 706.07).

In this regard, there are 5 independent claims in this application: claims 1, 6, 10, 15, and 19. Despite the fact that these claims each define unique and different subject matter, the Office Action (mailed May 15, 2006), which immediately preceded the present FINAL Office Action, rejected these claims as a group, stating:

> Referring to claims 1, 6, 10, 15, 19, Boyle teaches a method and a memory device interface comprising: determining at least one characteristic [see column 3, lines 45-48 and column 7, lines 8-19] of a first input/output (I/O) device [see figure 2, element 22] that is coupled to a memory device interface [see figure 2, element 80], the memory device interface being configured to enable data transfers between the I/O device and a memory device [see column 7, lines 37-43 'transfers'] and buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface [see figure 2, element 41], a size of the first portion being responsive to the at least one characteristic of the first I/O device [see column 7, lines 5-19, 37-43,59-62]; determining at least one characteristic [see column 3, lines 54-62 and column 7, lines 8-19] of a second I/O device [see figure 2, element 24] that is coupled to the memory device interface [see figure 2, element 80]; and buffering data corresponding to the second I/O device in a second portion of the buffer [see figure 2, element 42], a size of the second portion being responsive to the at least one characteristic of the second I/O device [see column 7, lines 5-19, 37-43, 59-62].

The substantive language quoted above, however, tracks only the language of claim 1 of the present application, does not address or mention unique elements of the other rejected claims. As such, Applicants substantively responded to this rejection, in connection with the arguments presented in support of the patentability of claim 1. As to the unique element of claim 6, 10, 15, and 19, which were not addressed in this rejection, however, Applicants were unable to adequately or fairly respond to the rejections. Indeed, in Applicants' prior response, Applicants pointed out to the Examiner that the language of

independent claims 6, 10, 15, and 19 each differ from the language of claim 1 (the only language addressed in the rejection), and requested that these claims be treated individually (as they should have been in the previous Office Action).

In the present (FINAL) Office Action, the Examiner has, in fact, addressed each of these remaining independent claims on an individual basis. Indeed, the language now quoted for each of these claims parallels the language of each claim. However, Applicant has not yet had a fair opportunity to properly develop the issues for appeal in these claims, as these new rejections have been made FINAL.

Consider the last element of claim 6 as an example. With respect to this last element, the FINAL Office Action states:

> wherein the buffering capacity of the first portion is responsive to at least one characteristic of a first I/O device that provides data to the memory device interface via the first data transfer link ***[see column 7, lines 5-19, 37-43, 59-62 and column 4, lines 32-60, which discloses that the system 20 differentiates element 22 and 24 from each other and that the host device can comprises a set-top box, a personal video recorder or other source of audiovisual information, this differentiation is made by determining a characteristic of both of the elements 22 and 24]***, and the buffering capacity of the second portion is responsive to at least one characteristic of a second I/O device that provides data to the memory device interface via the second data transfer link ***[see column 7, lines 5-19, 37-43, 59-62 and column 4, lines 32-60, which discloses that the system 20 differentiates element 22 and 24 from each other and that the host device can comprises a set-top box, a personal video recorder or other source of audiovisual information, this differentiation is made by determining a characteristic of both of the elements 22 and 24.]***"

(*Emphasis added.*) As can be readily verified, the rejection of claim 6 is now SIGNIFICANTLY different than the rejection of that claim set out in the previous Office Action. In fact, this is the first time during the prosecution of this application that the Examiner has advanced this argument. As such, Applicants have not had a fair

opportunity to consider and respond to this argument (either by argument or amendment). As the present Office Action has been made FINAL, the Applicants' ability to respond to this new argument by amendment (if appropriate) has been unduly restricted.

The FINAL Office Action has similarly advanced new substantive grounds for rejections with respect to independent claims 10, 15, and 19, which new grounds were not necessitated by any prior amendments made by Applicants.

Unfortunately, the pre-appeal conference panel denied Applicants' request for a pre-appeal conference, stating that the appropriateness of the FINALity of the rejection should instead be properly addressed by a petition. Accordingly, Applicants understand that this is not a substantive issue for the Board to decide on this appeal. However, the Board can consider the Examiner's diligence (or lack thereof) in hastening the prosecution of this application as reflective of the overall quality of Examination given to this application.

Rejections of Claims Under 35 U.S.C. §103(a) Should be Overturned

The FINAL Office Action rejected claims 11 and 16 under 35 U.S.C. § 103(a) as allegedly unpatentable over Boyle in view of Ward. These rejections should be overturned. In this regard, the Office Action admitted that Boyle "does not set forth the limitation of wherein the buffer comprises random access memory (RAM)," but alleges that this feature is taught by Ward. Applicants, however, disagree. As set forth above, the independent claims define over Boyle, and therefore claims 11 and 16 define over the Boyle/Ward combination for at least the same reasons.

In addition, the Office Action alleged that the combination of Ward with Boyle would have been obvious because "it was old and well known in the computer art to get the advantage of the ability of accessing data in random order by implementing the buffer using RAM." Applicants respectfully disagree.

This rationale is both incomplete and improper in view of the established standards for rejections under 35 U.S.C. § 103.

In this regard, the MPEP section 2141 states:

> Office policy has consistently been to follow *Graham v. John Deere Co.* in the consideration and determination of obviousness under 35 U.S.C. 103. As quoted above, the four factual inquires enunciated therein as a background for determining obviousness are briefly as follows:
>
> (A) Determining of the scope and contents of the prior art;
>
> (B) Ascertaining the differences between the prior art and the claims in issue;
>
> (C) Resolving the level of ordinary skill in the pertinent art; and
>
> (D) Evaluating evidence of secondary considerations.
>
> . . .
>
> BASIC CONSIDERATIONS WHICH APPLY TO OBVIOUSNESS REJECTIONS
>
> When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to:
>
> (A) The claimed invention must be considered as a whole;
>
> (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;
>
> (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention and
>
> (D) Reasonable expectation of success is the standard with which obviousness is determined.
>
> *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

The foregoing approach to obviousness determinations was recently confirmed by the United Stated Supreme Court decision in KSR INTERNATIONAL CO. V. TELEFLEX INC. ET AL. 550 U.S. ___ (2007)(No. 04-1350, slip opinion, p. 2), where the Court stated:

> In Graham v. John Deere Co. of Kansas City, 383 U. S. 1 (1966), the Court set out a framework for applying the statutory language of §103, language itself based on the logic of the earlier decision in Hotchkiss v. Greenwood, 11 How. 248 (1851), and its progeny. See 383 U. S., at 15–17. The analysis is objective:
>
> "Under §103, the scope and content of the prior art areto be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background the obviousness or nonobviousness of the subject matter is determined. Such secondary considerations as commercial success, longfelt but unsolved needs, failure of others, etc., mightbe utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented." Id., at 17–18.

Simply stated, the Office Action has failed to at least (1) ascertain the differences between and prior art and the claims in issue; and (2) resolve the level of ordinary skill in the art. Furthermore, the alleged rationale for combining the two references (i.e., because it "was old and well known in the computer art to get the advantage of the ability of accessing data in random order by implementing the buffer in RAM") embodies clear and improper hindsight rationale. For at least these additional reasons, Applicant submits that the rejections of claims 11 and 16 should be overturned.

CONCLUSION

Based upon the foregoing discussion, Applicant respectfully requests that the Examiner's final rejection of claims 1, 3-6, and 8-19 be overturned by the Board.

In addition to the claims of Appendix A, Appendix B attached hereto indicates that there is no evidence being attached and relied upon by this brief. Appendix C attached hereto indicates that there are no related proceedings.

Please charge Hewlett-Packard Company's deposit account 08-2025 in the amount of $500 for the filing of this Appeal Brief. No additional fees are believed to be due in connection with this Appeal Brief. If, however, any additional fees are deemed to be payable, you are hereby authorized to charge any such fees to deposit account No. 08-2025.

Respectfully submitted,

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VIII. CLAIMS - APPENDIX

1. A method comprising:

determining at least one characteristic of a first input/output (I/O) device that is coupled to a memory device interface, the memory device interface being configured to enable data transfers between the first I/O device and a memory device;

buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface, a size of the first portion being responsive to the at least one characteristic of the first I/O device;

determining at least one characteristic of a second I/O device that is coupled to the memory device interface; and

buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device.

2. (Canceled)

3. The method of claim 1, further comprising:

receiving data from the first I/O device via a first data transfer link; and

receiving data from the second I/O device via a second data transfer link.

4. The method of claim 1, further comprising:

receiving a first data unit from the first I/O device;

buffering the first data unit in the first portion of the buffer; and

transferring the first data unit to the memory device;

receiving a second data unit from the second I/O device;

buffering the second data unit in the second portion of the buffer; and

transferring the second data unit to the memory device.

5. The method of claim 1, wherein the at least one characteristic comprises at least one of:

a rate at which the I/O device is able to read data from the memory device;

a rate at which the I/O device is able to write data to the memory device;

a bandwidth of a link coupled between the I/O device and the memory device interface;

a size of a data unit that the I/O device reads from the memory device per read request;

a size of a data unit that the I/O device writes to the memory device per write request;

a tolerance that the I/O device has for a delay by the memory device interface in fulfilling a write request; or

a tolerance that the I/O device has for a delay by the memory device interface in fulfilling a read request.

6. A method for allocating buffer capacity in a memory device interface that is configured to transfer data between an input/output (I/O) device and a memory device, the method comprising:

buffering data received via a first data transfer link in a first portion of a buffer of the memory device interface;

buffering data received via a second data transfer link in a second portion of the buffer, a buffering capacity of the first portion being different than a buffering capacity of the second portion; and

wherein the buffering capacity of the first portion is responsive to at least one characteristic of a first I/O device that provides data to the memory device interface via the first data transfer link, and the buffering capacity of the second portion is responsive to at least one characteristic of a second I/O device that provides data to the memory device interface via the second data transfer link.

7. (Canceled).

8. The method of claim 6, further comprising:

receiving a first data unit from the first I/O device via the first data transfer link;

buffering the first data unit in the first portion of the buffer;

transferring the first data unit to the memory device;

receiving a second data unit from the second I/O device via the second data transfer link;

buffering the second data unit in the second portion of the buffer; and

transferring the second data unit to the memory device.

9. The method of claim 6, further comprising:

receiving a first data unit from the memory device;

buffering the first data unit in the first portion of the buffer;

transferring the first data unit to the first I/O device;

receiving a second data unit from the memory device;

buffering the second data unit in the second portion of the buffer; and

transferring the second data unit to the second I/O device.

10. A memory device interface that is configured to enable data transfers between an input/output (I/O) device, the memory device interface comprising:

a buffer;

a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data corresponding to a first I/O device; and

a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data corresponding to a second I/O device, a size of the first portion of the buffer being different than a size of the second portion of the buffer.

11. The memory device interface of claim 10, wherein the buffer comprises random access memory (RAM).

12. The memory device interface of claim 10, wherein the first plurality of registers comprises:

a first buffer allocation counter that specifies a buffer allocation value that is configured to enable data received from the first I/O device to be buffered in the first portion of the buffer; and

a second buffer allocation counter that specifies a buffer allocation value that is configured to enable data received from the second I/O device to be buffered in the second portion of the buffer.

13. The memory device interface of claim 12, wherein the value of the first buffer allocation counter is decremented responsive to a buffer allocation value being sent to the first I/O device.

14. The memory device interface of claim 13, wherein the value of the first buffer allocation counter is incremented responsive to data being read from the first portion of the buffer.

15. A memory device interface comprising:

a buffer;

a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data received via a first data transfer link; and

a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data received via a second data transfer link, a size of the first portion of the buffer being different than a size of the second portion of the buffer.

16. The memory device interface of claim 15, wherein the buffer comprises random access memory (RAM).

17. The memory device interface of claim 15, wherein the first data transfer link is coupled to a first input/output (I/O) device, and the second data transfer link is coupled to a second I/O device.

18. The memory device interface of claim 15, wherein the first plurality of registers comprises:

a first buffer allocation counter that is configured to enable data received via the first data transfer link to be buffered in the first portion of the buffer; and

a second buffer allocation counter that is configured to enable data received via the second data transfer link to be buffered in the second portion of the buffer.

19. A system comprising:

means for determining at least one characteristic of a first input/output (I/O) device that is coupled to a memory device interface, the memory device interface being configured to enable data transfers between the I/O device and a memory device;

means for buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface, a size of the first portion being responsive to the at least one characteristic of the first I/O device;

means for determining at least one characteristic of a second I/O device that is coupled to the memory device interface; and

means for buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device.

20. (Canceled)

IX. EVIDENCE - APPENDIX

None.

IX. RELATED PROCEEDINGS- APPENDIX

None.